CND 202
ADVANCED ANALOG BUILDING BLOCKS
2024

Course Description

This course aims to introduce the trainees to advanced analog building blocks. The course covers three main topics: data converters, timing circuits (PLLs), and power management. The topics include ADC/DAC, Switched Capacitor Circuits, SAR ADC: CDAC & Comparators, Pipelined ADC, Sigma delta modulators, DACs, PLL fundamentals and circuits, DLLs, Power Management ICs, bandgap reference circuits, linear regulators and LDOs, switched-capacitor power converters, industrial issues, and battery chargers.

- **Tools:**
  - Virtuoso
  - Spectre
  - Virtuoso Visualization
  - ADE assember editting (maestro)
  - Calibre (nmDRC, nmLVS, xRC)

Contact Hours

Credit Hours	Lecture Hours	Lab Hours	Student work	Total
6	24 (1.25x2)/week	21 (3x1)/week	48	93

Prerequisites

Introduction to Analog Electronics

Learning Outcomes

After successful completion of this course, the student will be able to:

1. Have a top-level understanding of communication circuits including modulators, analog multipliers, mixers, PLLs, as well as D2A and A2D converters.
2. Design and simulate efficient reference circuits and LDOs.
3. Use modern advanced CAD tools to design and simulate analog electronic circuits.

Course Materials

Textbook:

- Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of A Analog Integrated Circuit Design, 2nd Edition

- Tony Chan Carusone, David Johns, Kenneth Martin, nalog Integrated Circuits, 5th Edition, Wiley.
- Asad A. Abidi, Paul R. Gray, Robert G. Meyer, Integrated Circuits for Wireless Communications. 1st Edition, Wiley-IEEE Pres.
- Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits. 4th Ed, McGraw-Hill Education.
  References:
- Material derived from the IEEE Journal, Transactions, and the International Solid-state Circuits Conference (ISSCC) proceedings.

CAD Tools: Cadence flow including

- Virtuoso ADE suite
- Spectre
- Virtuoso Visualization
- ADE assembler editing (maestro)
- Calibre (nmDRC, nmLVS, xRC)

Course Project: By the end of this course the students are required to deliver a complete project (chosen from variety of proposals) assigned by the industry experts and university professors instructors.

Course Schedule

Week	Lecture	Lab
	Phase 1: Data converters	
1	1. Sampling and Quantization a. Nyquist criteria b. Frequency domain c. Anit aliasing d. Quantization noise e. Non-uniform sampling 2. Introduction to ADC/DAC + KPIs a. overview of types: flash, SAR, pipeline, sigma delta, cyclic b. ADC vs DAC c. Applications speed vs accuracy	Lab1: using cadence AHDL library, create model of sampling system, investigate effect of under-, Nyquist and oversampling, effect of anti aliasing, frequency spectrum of signals, quantization noise

	d. Static and dynamic performance metrics: DNL, INL, ENOB, Histogram, missing codes; SNR; SNDR, SFDR, power-speed FOMs	
2	3. Switched Capacitor Circuits a. Switches: transistors, transmission gate, charge compensation (dummy), bootstrap b. The capacitor, charge losses, bottom plate sampling c. Ideal SC circuit: constant charge, two phases d. Examples: SC amplifier, SC integrator, SC charge adder 4. SAR ADC: CDAC & Comparators a. SAR algorithm b. RDAC vs CDAC (speed vs power) c. Comparators: opamps as comparators, preamplifiers, strong arm latch, d. Topology pros and cons e. Layout and matching considerations (SAR DAC) f. ADC reference voltage generation	Lab 2: comparator design (specs pending)
3	5. Pipelined ADC a. Pipeline concept, conversion speed vs bit throughput b. Ideal 1 bit MDAC, need for redundancy, 1.5 bit MDAC c. Accuracy bottlenecks, effect of opamp d. Digital correction e. Resolution scaling f. Reference voltage generation 6. Sigma delta I a. Concept and application cases b. First order sigma delta modulator, operation, components	Lab 3: integrator design (specs pending)

	c. Time domain and frequency domain d. NTF and STF e. Discrete time and continuous time modulators	
4	7. Sigma delta II a. Second order modulators b. Nonlinear effects and stability c. Feedback and feedforward d. System level design example (matlab toolbox, online resources) e. Higher order modulators 8. DACs a. Applications b. Voltage vs current DACs c. RDAC: simple, r2r network, thermometer d. Current steering e. FIR DAC	Lab 4: design of 2-level current steering DAC or 5-bit CDAC
Phase 2: timing circuits (PLLs)		
5	1. Fundamentals 1 ○ Introduction to timing (clock domains, trees, synchronization, metastability, skews …) ○ Oscillator fundamentals ○ Stability ○ Root locus, bode plot ○ jitter, analysis, types ○ noise, phase noise, relation to jitter 2. Fundamentals 2 ○ LC, RC oscillators and ring oscillators ○ Digital and voltage-controlled oscillators (DCO/VCO) ○ ring oscillators ○ relaxation oscillators	Lab 5: design of LC oscillator and ring oscillator (specs pending)
6	3. Introduction to PLLs ○ Overview (functional block diagram) applications ○ Linear model (qualitative descripion of loop filter effect)	Lab 6: using cadence AHDL library and ideal model for charge pump design type 2 PLL that is capable of locking.

	○ Phase & frequency relation ○ Transfer function ○ Order & type 4. PLL System ○ Stability ○ Noise transfer function ○ Transient behavior ○ PLL components	
7	5. Phase detectors and Charge pumps ○ Bang-bang ○ TDC 6. Loop filter ○ Effect on performance ○ Analog vs digital	Lab 7: design of transistor level charge pump and phase detector (specs pending)
8	7. Frequency dividers ○ Integer n divider ○ Fractional divider ○ Sigma delta 8. DLLS	Lab 8: design of sigma delta fractional FD
Phase 3: Power Management ICs		
9	1. Introduction to PM and applications • The need for multi power supplies • Battery operated devices • Case study: mobile Phone • Effect of technology scaling • Function of PMIC • Discrete vs integrated PM systems • Performance Metrics,line transient, load transient, efficiency 2. Review on feedback and stability • Definitions • Stability criteria • Bode plots • Root locus • First, second and higher order systems	Lab 9: Using Cadence AnalogLib simulate the behaviour of a second order feedback system and investigate the stability in relation to time constants and inputs.

10	3. Bandgap reference voltage circuits • PTAT and CTAT • The bangap voltage of silicon • BiCMOS and CMOS implementation • Current mode bandgap circuits 4. Linear regulators • The Low Drop-Out voltage cirtcuit • LDO architectures, • LDO stability, • LDO efficiency	Lab 10: using an existing opamp circuit or the opmap macro model in the Cadence Basic library build and LDO and simulate its behaviour and evaluate performance and stability.
11	5. Switched-Capacitor Power Converters • basic introduction, • Slow-Switching Limit • Fast-Switching limit, • different topologies for step up/down • charge pumps • voltage multipliers 6. Inductor based power converters • Overview on DC-DC converters • buck architecture, • CCM and DCM operations, • stability study, • boost, • buck-boost, • other architectures	Lab 11: design of a buck-boost converter
12	7. Analog and digital controllers • Digital control basics • Dc boost converters • PWM modulators • Application scenarios • Comparison 8. Advanced topics • DVFS • Industrial issues (packaging, hot carrier injection, failure modes, heat dissipation, ESD) • LED drivers,	Lab 12: design of a charge pump

	• Li-ion battery chargers	